

# An Empirical Study of Crosstalk in VDSM Technologies

Shahin Nazarian, Massoud Pedram  
Dept. of EE-Systems, University of Southern California  
Los Angeles, CA 90089

Emre Tuncer  
Magma Design Automation  
Santa Clara, CA 95054

## ABSTRACT

We perform a detailed study of various crosstalk scenarios in VDSM technologies by using a distributed model of the crosstalk site and make a number of key observations about the crosstalk effects in VLSI circuits. As example of these observations, we report that the combination of one crosstalk event at some site and another crosstalk event at a different site in the transitive fan-out of the first site may cause a slowdown or speedup of the circuit by an amount that can significantly exceed the sum of crosstalk effects caused by each site in isolation. As another example, we report that the common assumption that zero skew between the input transitions of aggressor and victim lines causes the worst case crosstalk effect is not always valid, and therefore, optimization or test based on such an assumption may be invalid. We also demonstrate the non-monotone behavior of the crosstalk effect with respect to the skew between the input transition of aggressor and victim lines. This work provides a first step toward the development of a new framework for timing analysis and test development in the presence of crosstalk events.

## Categories and Subject Descriptors

B.8.2 [Performance and Reliability]: Performance Analysis and Design Aids.

## General Terms

Algorithms, Design, Measurement, Performance, Theory.

## Keywords

Automatic test pattern generation (ATPG) tool, Crosstalk induced slowdown and speedup, Skew, Static timing analysis (STA), Transition time.

## 1. INTRODUCTION

The drastic down scaling of layout geometries in very deep submicron (VDSM) technologies along with the increase in the operational frequency of VLSI circuits have resulted in the aggravation of capacitive crosstalk effects. Timing analysis is an essential aspect of determining whether a crosstalk event can create a faulty output in a circuit. In particular, the signal arrival times and transition times (inverse of slew rates) in a circuit can change as a function of the crosstalk noise that is present in the circuit. Therefore, the accuracy of timing analysis tools strongly depends on the accuracy of arrival time and transition time calculations in the presence of crosstalk noise.

Crosstalk effect has been studied by using lumped RC models [1-4]. However, this model is inaccurate for global interconnects,

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.  
GLSVLSI'05, April 17-19, 2005, Chicago, Illinois, USA.  
Copyright ACM 1-59593-057-4/05/0004...\$5.00.

especially at high clock frequencies. Using a distributed coupling capacitance model produces more accurate and realistic results. Closed form formulas by using  $2\pi$  and  $4\pi$  configurations (which are based on linear circuit models) have been developed in [5] and [6], respectively.

However the quality of STA and ATPG tools degrades when using linear equations to model the nonlinear behavior of drivers. In [7,8] distributed RC modeling has been used to estimate the pulse induced by crosstalk effect. Several interesting properties have been reported in [9] for weak spot defects in the presence of crosstalk noise by using distributed RC modeling to simulate their interactions.

In this paper we perform extensive simulations by using distributed RC modeling of a crosstalk site and report a number of important properties of the crosstalk that may be exploited in STA and ATPG tools to increase the accuracy of crosstalk effect analysis and reduce the computational time of these tools. We also investigate the sensitivity of the delay and transition time of the output a crosstalk site to parameters such as its coupling capacitance value, the input skew between, and transition times of the inputs of the crosstalk site drivers.

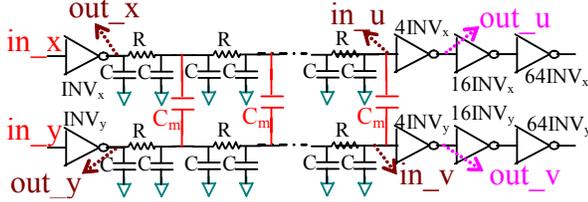
In this paper, we adopt the standard definition of arrival time and transition time that is commonly used in STA and ATPG tools, meaning that the *arrival time* of a signal transition is set to the time instance at which signal waveform crosses the 0.5V<sub>dd</sub> voltage level whereas the *transition time* of a signal transition is defined as the slope of a line connecting two specific points on the noisy input: the points are when the signal waveform crosses the 0.1V<sub>dd</sub> and 0.9V<sub>dd</sub> voltage levels. The *skew* between two signal transitions is the difference between their arrival times.

We use the configuration depicted in Figure 1 for all experiments. In this configuration, the inverter 4INV<sub>x</sub> is fed by a long interconnect line that is a potential crosstalk victim.<sup>1</sup> Aggressor and victim lines run parallel to each other and are 1000 $\mu$ m long and 0.200 $\mu$ m wide modeled by 10 stages of a RC- $\pi$  structure. We use standard inverter gates in TSMC 0.13 $\mu$  technology. The sheet resistance of metal interconnect in this technology is 0.074000 $\Omega$ /square. This value is used for each line (total line resistance is 370 $\Omega$ .) The unit line capacitance is 22.6 pF/meter; therefore, the total self capacitance (capacitance to the ground) of each line is 22.6fF. The total coupling capacitance between the two lines is changed from 0 to 300fF in our experiments (i.e.,  $C_m$  is set to values between zero and 30fF capturing different wire spacing.)<sup>2</sup> From now on, we will refer to INV<sub>x</sub> and INV<sub>y</sub> as the *line drivers*. Similarly, 4INV<sub>x</sub> and 4INV<sub>y</sub> will be called the *line receivers*. We will refer to out<sub>x</sub> and out<sub>y</sub> (in<sub>u</sub> and in<sub>v</sub>) as the near-end (far-end) of the lines. Either line can be considered as a victim when the other is an aggressor. However, from now on, we will treat line with input in<sub>x</sub> and output out<sub>u</sub> as the *victim line* and the other as the *aggressor line*.

<sup>1</sup> The size of eINV<sub>f</sub> is  $e$  times as big as that of INV<sub>f</sub>, where  $e$  can be 1, 4, 16, and 64 and  $f$  can be  $x$  and  $y$ .

<sup>2</sup> We have performed all of these experiments with TSMC 0.25 $\mu$ m process technology and found similar outcomes. In this paper, we report only the results for TSMC 0.13 $\mu$ m.

We define the (normalized) *sensitivity* of variable  $p$  to variable  $q$  as  $\sigma = (q \cdot \Delta p) / (p \cdot \Delta q)$ . We say  $p$  is *insensitive* to  $q$ , exactly when  $\sigma = 0$ ; furthermore,  $p$  is *weakly sensitive* to  $q$  exactly if  $0 < \sigma < 1$ ; otherwise we say that  $p$  is *highly sensitive* to  $q$ . At times we will refer to  $\Delta p$  as *slowdown* or *speedup* of  $p$  depending on whether  $\Delta p$  is positive or negative, respectively. We will also use the term *crosstalk-aware delay and transition time* of node  $p$  to refer to the delay and transition time of that node when the impact of crosstalk capacitances are considered.



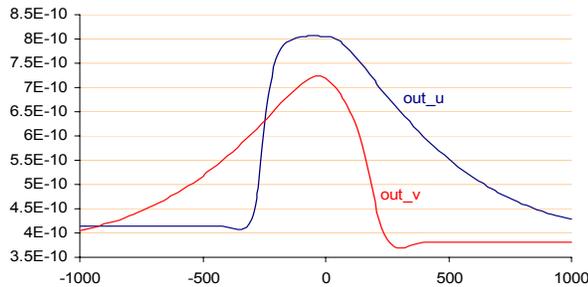
**Figure 1: The crosstalk model for long parallel lines. The configuration used in our experiments.  $R=3.7\Omega$ ,  $C=1.13fF$ .**

The remainder of this paper is organized as follows. Sections 2 and 3 focus on the slowdown effect of the crosstalk. More precisely, in section 2, we investigate the sensitivity of the crosstalk-aware delay and transition time of the output of the victim line driver to the input skew whereas, in section 3, we study the sensitivity of those to the transition time of the inputs of the victim line and aggressor line drivers. Section 4 deals with crosstalk speedup effect. The interaction of crosstalk sites is discussed in Section 5. Concluding remarks are provided in Section 6.

## 2. DEPENDENCE ON INPUT SKEW

### 2.1 Output Slowdown vs. Input Skew

To study the sensitivity of the crosstalk-aware output delay to input skew, we create signal transitions with opposite directions at the inputs of line drivers, namely  $in_x$  and  $in_y$ . The signal transitions of both lines will be slowed down. We set the arrival time of a falling transition at  $in_y$  to 1000 ps and sweep the arrival time of a rising transition at  $in_x$  from -1000 to +1000 ps; therefore the input skew between  $in_x$  and  $in_y$  changes from -1000ps to +1000ps. We also set their transition times to 100ps. Both  $out_u$  and  $out_v$  exhibit a crosstalk-induced slowdown in this case. Figure 2 shows the slowdown of  $out_u$  (delay of  $out_u$  w.r.t.  $in_x$ ) and  $out_v$  (delay of  $out_v$  w.r.t.  $in_y$ ).<sup>3</sup> Coupling capacitance is 300fF ( $C_m=30fF$ .) An inverter cell with nearly equal fall and rise time ratio is used for all INV cells in the configuration, therefore in Figure 2 the maximum slowdown at  $out_u$  and  $out_v$  has less than around 75ps difference.



**Figure 2: Delay from  $in_x$  ( $in_y$ ) to  $out_u$  ( $out_v$ ) vs. input skew between  $in_x$  and  $in_y$ .**

<sup>3</sup> In all figures presented in this paper, the x-axis is in units of ps whereas the y-axis data is in units of s.

**P1:** Crosstalk-aware delay can be highly sensitive to the input skew. Especially, for skew values that are close to the one generating the worst-case delay, a small change in the skew can significantly change the delay.

For example in Figure 2, a 25ps change in the input skew can change the delay of transition at  $out_u$  for more than 105ps. P1 highlights the importance of accurately computing the arrival time of signal transitions at circuit lines in the presence of crosstalk noise.

**P2:** The worst-case crosstalk slowdown at the output of the victim line receiver occurs at a certain skew, but a significant slowdown (e.g., more than 20% delay increase) occurs with a large range of skews.

One way to reduce the crosstalk effect of a site is to deliberately change the delay of circuit lines driving the corresponding victim and/aggressor lines (e.g. by using buffers.) This can change the input skew such that the slowdown created by that crosstalk site cannot create any error. P2 shows that in order to significantly reduce the slowdown from its worst-case level, the input skew will have to be changed by a rather large amount.

There is a common belief that is relied on in crosstalk fault models [2,10], ATPG tools [3,11], and STA tools [12,13]. According to this view, the worst case slowdown of a crosstalk event occurs precisely when the aggressor and victim line inputs switch simultaneously, i.e., the inputs have zero skew transitions. This concept is mainly a consequence of using a lumped capacitive model for studying the crosstalk effects. However, Figure 2 (also Figure 6) shows that this concept may not be true even for two completely symmetric interconnects, i.e., with the same lengths, drivers and receivers, output loads (fan-out), and input transition times. Our experiments confirm that even a zero skew between transitions at the near-end of the lines, i.e.,  $out_x$  and  $out_y$ , may not necessarily create the worst-case crosstalk-induced slowdown. The reason is that the crosstalk coupling of the aggressor and victim lines is distributed along the length of the lines and the crosstalk effect at one point of the victim line propagates and affects the subsequent points along the victim line. Therefore, the crosstalk effect at each point of the victim line is the summation of coupling effects of that point plus the delayed effects propagated from the preceding points. As a result, the maximum crosstalk slowdown occurs over a much wider window of time than is usually assumed (refer to P2.)

**P3:** The maximum crosstalk slowdown does not necessarily occur for zero input skew condition even for completely symmetric interconnects.

P3 provides motivation for establishing a framework for alignment of multiple aggressors and the victim line such that the worst-case crosstalk effect is generated. An algorithm is suggested in [14] to solve the multiple aggressor alignment problems. Unfortunately, this algorithm is based on lumped modeling of crosstalk coupling.

#### 2.1.1. Slowdown effect at the far-end of the victim line.

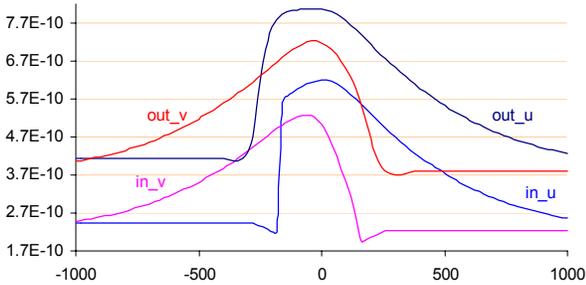
In Figure 3 we report the slowdown of  $in_u$  ( $in_v$ ) w.r.t.  $in_x$  ( $in_y$ ) and compare this slowdown with results of Figure 2 (slowdown of  $out_u$  ( $out_v$ ) w.r.t.  $in_x$  ( $in_y$ )).

**P4:** Delay at the output of the victim line receiver,  $out_u$  ( $out_v$ ), follows the shape of delay at the far-end of the victim line,  $in_u$  ( $in_v$ ).

### 2.2 Output Transition Time vs. Input Skew

A new experiment similar to the one described in Section 2.1 is set up. The only difference is that now the transition time change at the interconnect output ( $out_u/out_v$ ) due to the crosstalk effect is

simulated. Figure 4 shows the dependence of transition time of out\_u and out\_v on the input skew. The following summarizes the observations made from this experiment.



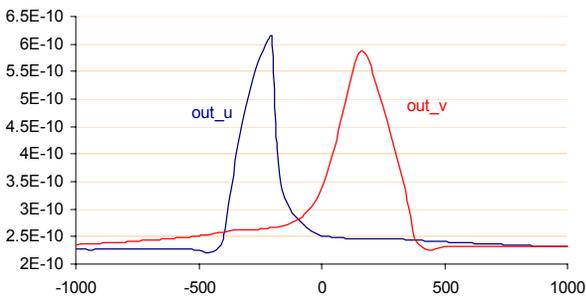
**Figure 3: Delay from in\_x (in\_y) to in\_u (in\_v) and from in\_x (in\_y) to out\_u (out\_v) vs. input skew.**

**P5:** The output transition time can be highly sensitive to the input skew. Especially, for skew values that are close to the one generating the worst-case increase in transition time, a small change in the skew can significantly change the transition time.

For example in Figure 4 less than 20ps change in skew can result in more than 200ps increase in the transition time of out\_u.

**P6:** The maximum transition time at the output of the victim line occurs for a certain input skew, with a significant increase in transition time occurring for a large range of input skew values.

**P7:** The maximum transition time at the output of the victim line receiver does not occur for the zero input skew even for completely symmetric interconnects.



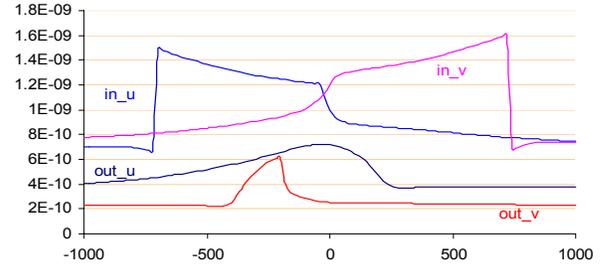
**Figure 4: Transition times of out\_u and out\_v vs. input skew.**

### 2.2.1. Transition time change at the far-end of the victim line

In Figure 5 we compare the transition time of the signal transitions at the far-end of the victim line, i.e., in\_u (in\_v) with that of the output of the victim line receiver, i.e., out\_u (out\_v). In contrast to what we observed in Figure 3 for slowdown, the transition time comparison shows different characteristics.

**P8:** Transition times of the transitions at the far-end and the output of the victim line receiver are very different in terms of their waveform characteristics.

In general the transition at the input of a gate tends to be smoothed out, and hence, the transition at the gate's output will not change as drastically as the change in the gate's input transition.

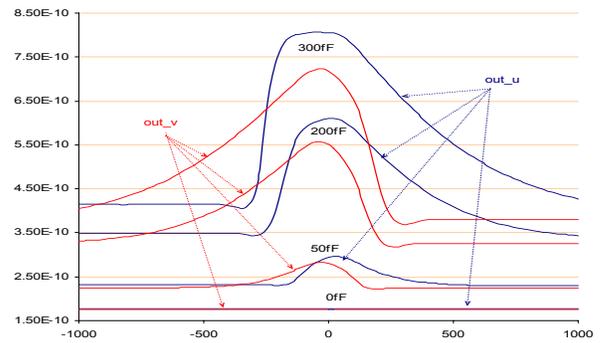


**Figure 5: Transition times of in\_u (in\_v) and out\_u (out\_v) vs. input skew.**

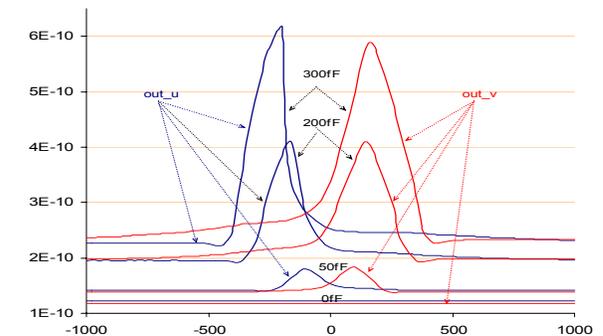
### 2.3 Crosstalk Delay-Aware Sensitivity to the Coupling Value

We ran the experiment described in Section 2.1 with different values for the coupling capacitance. Figure 6 shows the slowdown at the outputs, out\_u and out\_v, vs. the input skew for different coupling values. Figure 7 shows the corresponding data of the transition time.

**P9:** Both slowdown and transition time at the output of the victim line receiver are highly sensitive to the coupling capacitance value.



**Figure 6: Delay from in\_x (in\_y) to out\_u (out\_v) vs. input skew between in\_x and in\_y for different coupling values.**



**Figure 7: The transition times of out\_u and out\_v vs. input skew for different coupling values.**

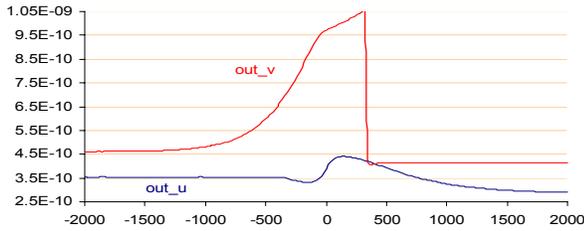
**P10:** The input skew values that cause the maximum slowdown and largest transition time at the output of the victim line receiver change with the coupling capacitance value.

P10 highlights the importance of the coupling value on determining the input skew values that give rise to the worst case slowdown and largest transition time, respectively.

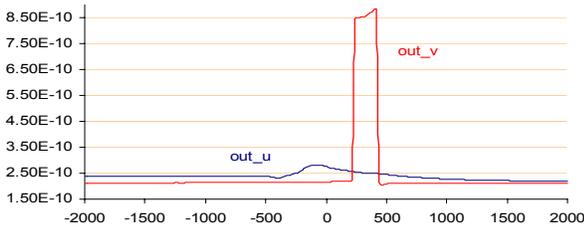
## 2.4 Unbalanced Cells

So far we reported experiments on configurations with inverter cells with nearly equal rise and fall times. We call these cells *balanced*. To see how different rise and fall times may affect the results, we use driver and receiver inverter cells with different pulldown and pullup strengths. We refer to these types of logic gates as *unbalanced* cells. Figures 8 and 9 show the delay and transition time change vs. input skew similar to configuration of Figures 2 and 3 respectively, but with unbalanced cells used as line drivers and receivers. The falling transition at  $in_y$  occurs at +2000ps whereas the rising transition at  $in_x$  occurs between 0 to +4000ps, i.e., the input skew changes from -2000ps to +2000ps. The delay value for very large negative or positive skews actually captures the delay of the interconnect output which is not affected by any crosstalk. For example, the delay of  $out_u$  for the skew of -2000ps is around 470ps and that for the skew of +2000 ps is around 410ps. The difference between the two delay values is the delay of an interconnect line that is influenced by the voltage level of the other interconnect through the coupling capacitance.

**P11:** Crosstalk-aware delay and transition time at the output of the victim line receiver are highly sensitive to the ratio of pull-up and pull-down strengths of the inverter cells.



**Figure 8:** Delay from  $in_x$  ( $in_y$ ) to  $out_u$  ( $out_v$ ) vs. input skew using an unbalanced cell.



**Figure 9:** Transition times of  $out_u$  and  $out_v$  vs. input skew for an unbalanced cell.

Figure 8 contains interesting data to show that the assumption that zero input skew results in maximum crosstalk effect is indeed a misconception (cf. P3.) Assume a test generator which works based on this zero input skew assumption, finds a test that excites zero skew input transitions at the input of the crosstalk site with slowdown vs. skew curves in Figure 8. Assume that if a circuit generates less than 960ps slowdown at that crosstalk site it passes the test. Now, based on the zero input skew assumption, the circuit passes the test but in fact if the test generator had applied input excitations with a skew of around 300ps, then the crosstalk error would have been observed.

Figure 8 also points out a fact about crosstalk, which we refer to as the non-monotone property of the crosstalk effect. Assume that the arrival time of  $in_x$  is sped up (e.g., as a result of the speedup effect of a crosstalk site in the transitive fan-in of node  $in_x$ ) such that the input skew between  $in_x$  and  $in_y$  is reduced from 400 to 300ps. This skew reduction creates a 650ps increase in the crosstalk-induced slowdown at  $out_v$ . Now, looking at the same scenario in the opposite

direction, we can see that an input skew increase from 300 to 400ps will reduce the delay at  $out_v$  by 650ps. So, in general, circuit scenarios can be found such that a speedup at the input line of a crosstalk site can result in either a speedup or a slowdown effect at the output of the site. Similarly, an input slowdown may cause an output slowdown or output speedup. In Section 5 we will further explore the impact of this non-monotone behavior when the crosstalk sites interact with one another.

**P12:** Crosstalk effect exhibits a non-monotone behavior with respect to the skew between the arrival times of the inputs of the aggressor and victim line drivers.

## 3. DEPENDENCE ON TRANSITION TIME

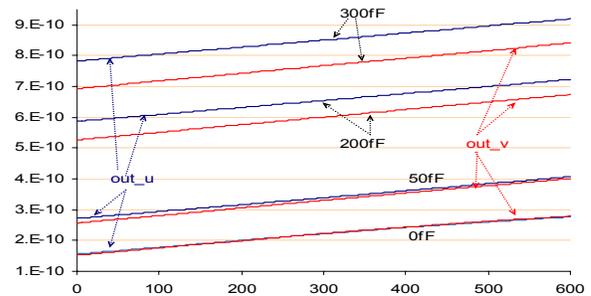
To study the effect of transition time of signals at the input of the victim line driver and/or the aggressor line driver, we keep the skew between the transitions at  $in_x$  and  $in_y$  fixed at zero. We apply a falling transition at  $in_y$  and a rising transition at  $in_x$  with identical arrival times so that both  $out_u$  and  $out_v$  will experience crosstalk-induced slowdown. We consider a reasonable range of transition times from 0 to 600ps.

We will consider two scenarios for the transition time change. In the first scenario, the transition times of both  $in_x$  and  $in_y$  are changed. In the second scenario, only one of the input transition times is changed while the other one is kept constant. A balanced inverter cell has been used for both INV cells in the configuration of Figure 1.

### 3.1 Both Input Transition Times Change

The transition time of  $in_x$  and  $in_y$  are identical and vary in lockstep from 0 to 600ps. Figure 10 illustrates how the slowdown of the transitions at  $out_u$  and  $out_v$  change based on change of transition times of  $in_x$  and  $in_y$ . It is seen that a 600ps increase in input transition time of both  $in_x$  and  $in_y$  causes only a 145ps slowdown for  $out_u$  (with a coupling capacitance value of 300fF.) Therefore, assuming equal transition times for the aggressor and victim inputs, the slowdown at the output of the victim line receiver is only weakly sensitive to its input transition time.

Comparing P12 with P1, we conclude that crosstalk-aware delay sensitivity to the input transition time is much lower than that to the input skew. This has the implication that, as far as crosstalk is concerned, the accuracy of arrival time computation is more important than the accuracy of transition time computation. Figure 11 illustrates how the transition time of the transition at the output of the crosstalk site, i.e.  $out_u/out_v$  would change when transition times of both  $in_x$  and  $in_y$  change. From this figure, a 600ps increase in the input transition time of both  $in_x$  and  $in_y$  changes the transition time at  $out_v$  by only 10ps.



**Figure 10:** Delay from  $in_x$  ( $in_y$ ) to  $out_u$  ( $out_v$ ) vs. input transition time (both transition times change) for different coupling capacitance values.

### 3.2 Only One Transition Time Changes

We simulate the crosstalk effect by keeping transition time of the signal transition at  $in_y$  constant at 100ps and then changing transition time of  $in_x$  from 0 to 600ps. Other parameters have been set similar to those of the experiment reported in Section 3.1. Figure 12 shows the effect of transition time change at one input ( $in_x$ ) on the slowdown seen at the outputs.

Considering  $in_y$  and  $out_v$  as the input and output of the victim line, there will be less slowdown at  $out_v$  if the transition time at the input of the aggressor line driver,  $in_x$ , increases.

**P13:** Crosstalk-aware delay and transition time of the output of the victim line are only weakly sensitive to its input transition time.

**P14:** For a given transition time at input of the victim line driver, faster aggressor causes larger worst-case slowdown.

**P15:** The maximum slowdown occurs when the victim has the largest transition time whereas the aggressor has the smallest transition time.

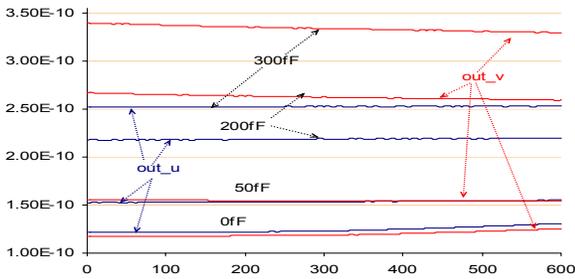


Figure 11: Transition times of  $out_u$  and  $out_v$  vs. input transition time (both change) for different coupling capacitance values.

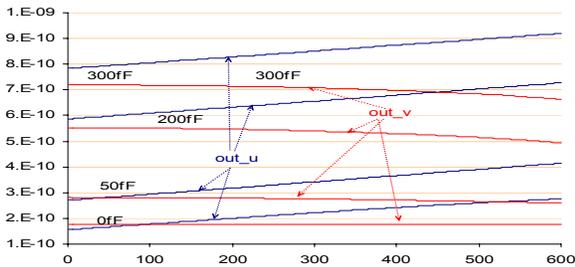


Figure 12: Delay from  $in_x$  ( $in_y$ ) to  $out_u$  ( $out_v$ ) vs. transition time of  $in_x$  for different coupling values.

Table 1 lists the slowdown for several interesting transition times taken from Figure 10 and Figure 12. In the last row, the slowdown values for the last three columns (664, 718, and 720) substantiate P14. Comparing the second column entry (920) with entries of columns 1, 3 and 4 (919, 805, and 785) substantiates P15. In Figure 13 we study a similar effect to what was presented in Figure 11. However, only transition time at  $in_x$  is changed.

**P16:** Slower aggressor creates slower transitions at the output of the victim line receiver.

Table 1: Crosstalk-aware delay sensitivity to the input transition time (in ps.)

transition time( $in_x$ )	600	600	100	0
transition time( $in_y$ )	600	100	100	100
delay( $out_u$ )	919	920	805	785
delay( $out_v$ )	841	664	718	720

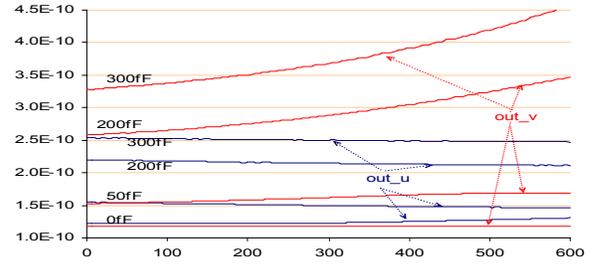


Figure 13: Transition time  $out_u$  ( $out_v$ ) vs. transition time of  $in_x$ .

## 4. CROSSTALK-INDUCED SPEEDUP

To study the crosstalk-induced speedup effect, we consider transitions with the same direction of change at inputs,  $in_x$  and  $in_y$ . We set the arrival time of a rising transition at  $in_y$  to 1000 ps and sweep the arrival time of a rising transition at  $in_x$  from -1000 to +1000 ps; therefore the input skew between  $in_x$  and  $in_y$  changes from -1000ps to +1000ps. We also set the input transition times to 100ps. Figure 14 illustrates the speedups that occur at outputs,  $out_u$  and  $out_v$  based on the input skew change. Figure 15 illustrates the output transition time vs. the input skew for the speedup case.

Having compared Figure 14 with Figure 2, we find that the maximum speedup at the victim's output is 233ps whereas the maximum slowdown was 390ps. Figure 3 and Figure 15 shows that the maximum decrease in transition time at the victim's output is 110ps whereas the maximum increase in transition time for the slowdown case was 390ps. Hence, the amount of speedup for the same configuration is lower than the slowdown and the transition time change in the speedup case is less than that in the slowdown case.

Since both lines make transitions in the same direction, the  $out_u$  and  $out_v$  curves are symmetric to each other. Other observations are similar to those of the slowdown ones.

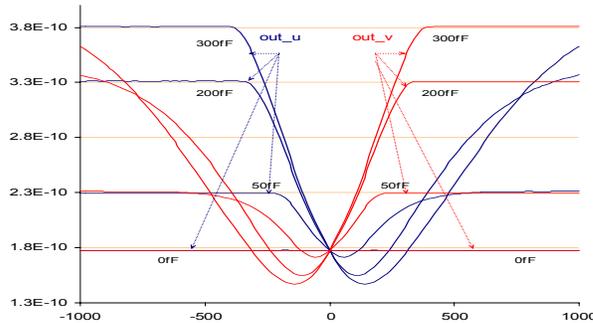


Figure 14: Delay from  $in_x$  ( $in_y$ ) to  $out_u$  ( $out_v$ ) vs. input skew for different coupling values for the speedup case.

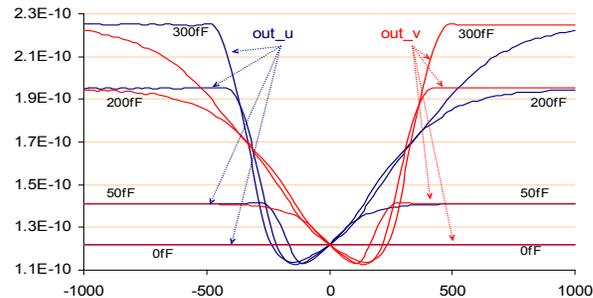


Figure 15: Transition time of  $out_u$  and  $out_v$  vs. input skew for different coupling values for the speedup case.

Figures 14 and 15 show that even for transitions in the same direction the zero skew may not create the worst case slowdown or output transition time. So P3 and P7 must be true even for completely balanced cells with equal rise and fall time transitions.

## 5. INTERACTION OF SITES

The crosstalk induced speedup or slowdown effects of two crosstalk sites, each similar to the one shown in Figure 1, may interact with each other if one is in the transitive fan-out of the other. In this section we show this interaction can generate a total delay effect that is more significant than the delay effects caused by each site in isolation.

### 5.1 Interaction of Two Slowdown Effects

Assume each has a total coupling value of 300fF. Assume both sites use the same fairly balanced cell that was used in Section 2.1 for all INV cells in the model. Consider a falling and a rising transition at the inputs in\_x and in\_y of the first crosstalk site. Figure 6 showed the slowdown effect vs. skew for this site. From Figure 6 a 30ps decrease in the arrival time of the transition at in\_x of the first crosstalk site, which is equivalent to a 30ps increase in its input skew, can result in a slowdown of 150ps at out\_u of this site. Let's consider a worst-case scenario where all of this slowdown effect will reach the input of the second crosstalk site. Referring to Figure 6, a 150ps change in input skew can cause an output slowdown of up to 400ps. Therefore the total slowdown along the path is 30+150+400 or 580ps. If we study the slowdown effect of the crosstalk sites one at a time, then we will incorrectly conclude that a 30ps change in the input skew of the site will create 150ps slowdown on each site, and thus to the total slowdown of the path is 30+150+150 or 330ps. Therefore, separate worst-case analysis of the two crosstalk sites would underestimate the total path slowdown by 93%. In addition, we should take into account the transition time change created at the output of the crosstalk sites. For example, in the case that one crosstalk site directly feeds into the other, from Figure 7, a 30ps change in the input skew causes a 90ps transition time change at the output of the first site and input of the second site. This in turn creates around 30ps extra slowdown at the output of the second site. This means that the total path slowdown is actually 580+30 or 610ps.

**P17:** Crosstalk sites along a path may result in a significant increase in circuit delay, which can be much higher than the summation of delay increases caused by each site individually.

### 5.2 Interaction of Slowdown and Speedup Effects

Assume a first site with total coupling value of 50fF uses the same fairly balanced cell that was used in Section 2.1 for all INV cells in the model. Assume rising transitions at the inputs of in\_x and in\_y of the first crosstalk site. Figure 14 showed the speedup effect vs. skew for this site. A 240ps decrease in the arrival time of the transition at in\_x of the first site, which is equivalent to a 240ps increase in the input skew, can in the worst case cause a 60ps speedup at the output of the site. This speedup is in turn equivalent to a decrease in the input skew of the second site that is in the transitive fanout of the first one. The second site has a total coupling value of 300fF. It uses the unbalanced cell used in Section 2.4. Therefore, from Figure 10, a 60ps decrease in the input skew can create up to 650ps increase in slowdown. Therefore the total slowdown along the path is 240-60+650 or 830ps. Studying the second site in isolation, a 240ps increase in the input skew of the second site, which from Figure 8 means no slowdown at the output of this site, could be generated by the second site if the first site did not exist. The total slowdown created by each site in isolation is 240-60=220ps. Therefore the total slowdown caused by the interaction of site is more than 3.7 times as

large as the summation of crosstalk effects in isolation. This example highlights the non-monotone behavior of crosstalk site described in P12.

The key to the synergistic interactions discussed in 5.1 and 5.2 is that crosstalk-aware delay is highly sensitive to the input skew (refer to properties P3 and P4.)

## 6. CONCLUSIONS

We presented the properties found from our extensive simulations of crosstalk-induced slowdown and speedup effects in TSMC 0.13μ process technology. The distributed modeling of capacitive coupling was used to create more realistic results compared to the previous work in the literature and industry. We reported that the sensitivity of crosstalk-aware delay and transition time of the output of victim line receiver to the input skew is much higher than that to input transition times (P1, P5, and P13.) We also showed that the concept of zero skew used in ATPG tools for post-silicon testing and characterization, and pre-silicon validation may fail (P3 and P7.) We have identified scenarios where the interaction of two crosstalk sites creates delay effects well in excess of the sum of their individual delay effects (P17.) Our long term goal is to make use of these findings to improve the accuracy of static timing analysis tools.

## 7. REFERENCES

- [1] A. Rubio, N. Itazaki, X. Xu, K. Kinoshita, "An approach to the analysis and detection of crosstalk faults in digital VLSI circuits," *Tran. Comp.-Aided Design of Integ. Cir. & Sys., Vol. 13*, pp. 387-395, 1994.
- [2] W. Chen, S.K. Gupta, M.A. Breuer, "Analytic models for crosstalk delay and pulse analysis under non-ideal inputs," *Proc. Int'l Test Conf. (ITC)*, pp. 809-818, 1997.
- [3] W.Y. Chen, S.K. Gupta, M.A. Breuer, "Analytical models for crosstalk excitation and propagation in VLSI circuits," *Trans. On Computer-Aided Design of Integ. Cir. & Sys., Vol. 21 No. 10*, pp. 1117-1131, 2002.
- [4] C. Tsai, M. Marek-Sadowska, "Modeling crosstalk induced delay," *Proc. Int'l Symp. on Quality Electronic Design (ISQED)*, pp. 189-194, 2003.
- [5] J. Cong, D. Pan, P.V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization," *Proc. Asia South Pacific Design Automation Conf. (ASP-DAC)*, pp. 373-378, 2001.
- [6] M.R. Becker, D. Blaaw, V. Zolotov, R. Panda, I.N. Hajj, "Analysis of noise avoidance techniques in DSM interconnects using a complete crosstalk noise model," *Proc. Design, Automation, & Test Eur. (DATE)*, pp. 456-463, 2002.
- [7] K. Agarwal, Y. Cao, T. Sato, D. Sylvester, C. Hu, "Efficient generation of delay change curves for noise-aware static timing analysis," *Proc. Asia South Pacific Design Automation Conf. (ASP-DAC)*, pp. 77-84, 2002.
- [8] P. Heydari, M. Pedram, "Analysis and reduction of capacitive coupling noise in high-speed VLSI circuits," *Proc. Int'l Conf. on Computer Design (ICCD)*, pp. 104-109, 2001.
- [9] S. Irajpour, S. Nazarian, L. Wang, S.K. Gupta, M.A. Breuer, "Analyzing crosstalk in the presence of weak bridge defects," *Proc. VLSI Test Symp. (VTS)*, pp. 385-392, 2003.
- [10] S.T. Zachariah, Y. Chang, S. Kundu, C. Tirumurti, "On modeling crosstalk faults," *Proc. Design, Automation & Test Eur. (DATE)*, pp. 490-495, 2003.
- [11] W.Y. Chen, S.K. Gupta, M.A. Breuer, "Test generation for crosstalk induced delay in integrated circuits," *Proc. Int'l Test Conf. (ITC)*, pp. 191-200, 1999.
- [12] P. Chen, D.A. Kirkpatrick, K. Keutzer, "Switching window computation for static timing analysis in presence of crosstalk noise," *Proc. Int'l Conf. on Computer-Aided Design (ICCAD)*, pp. 331-337, 2000.
- [13] I. Huang, S.K. Gupta, M.A. Breuer, "Accurate and efficient static timing analysis with crosstalk," *Int'l Conf. on Computers and Processors (ICCD)*, pp. 265-272, 2002.
- [14] S. Sirichotiyaku, D. Blaauw, C. Oh, R. Levy, V. Zolotov, J. Zuo, "Driver modeling and alignment for worst-case delay noise," *Proc. Design Automation Conf. (DAC)* pp. 720-725, 2001.