Battery-Powered Digital CMOS Design

Abstract — *In this paper we study tradeoffs between energy dissipation and delay in battery-powered digital CMOS designs. In contrast to previous work, we adopt an integrated model of the VLSI circuit and the battery sub-system that powers it. We show that accounting for the dependence of battery capacity on the average discharge current changes shape of the energy-delay trade-off curve and hence the value of the operating voltage that results in the optimum energy-delay product for the target circuit. Analytical derivations as well as experimental results demonstrate the importance of correct modeling of the battery-hardware system as a whole and provide a more accurate basis for comparing various low power optimization methodologies and techniques targeted toward battery-powered electronics. Finally, as an example application, we consider the problem of optimal battery selection for a given VLSI circuit.*

I. INTRODUCTION

Due to rapid progress in the semiconductor process technology, the device density and operating frequency have greatly increased, making power consumption in digital circuits a major design concern. High power consumption reduces the battery life in portable devices. The goal of low-power design for battery-operated devices is to extend the battery lifetime while meeting the required performance specification.

The most effective method for low-power design is to reduce the supply voltage and compensate for the performance loss by a combination of architectural and circuit optimization techniques. *Static voltage scaling* [1][2] and *dynamic voltage scaling* [3] techniques have been proposed. It is important to evaluate the proposed techniques by using appropriate metrics, i.e., power, energy, delay, or energy-delay product. These metrics can be used in different applications (depending on the design requirements) to guide optimizations toward the best solution. It has been argued in [2] that the energy-delay product is more relevant for the purpose of comparing various low power design methodologies and techniques.

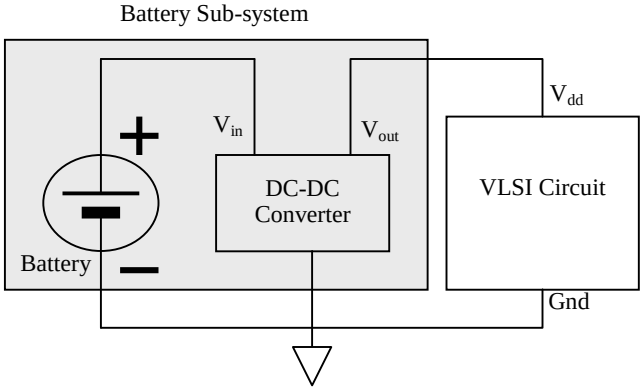

Figure 1 A complete battery operated system

As shown in Figure 1, a battery-powered digital system (which is typically present in portable electronic devices such as cellular phones, notebook computers, PDA's) consists of the VLSI circuit, the battery cell, and the DC-DC converter. Although low-power design for portable electronics aims at extending the battery life, discussions of low-power-design metrics have entirely focused on the VLSI circuit itself, assuming that the battery system is an ideal source that outputs a constant voltage and stores/delivers a fixed amount of energy [4]. However, in reality, the energy stored in a new *primary* (non-rechargeable) battery or a fully charged *secondary* (rechargeable) battery cannot be extracted/used to the full extent. In fact, in some cases, even 50% energy delivery is not possible. This phenomenon is caused by the fact that the "effective capacity" of the battery depends strongly on the mean value of the current discharged from the battery. More precisely, a higher portion of the total battery capacity is wasted at higher discharge current. High rate (current) discharge can indeed cause dramatic (more than 50%) waste of the initial capacity (energy) of the battery [6].

We will show that, for a given battery, the amount of energy that can be used by the VLSI circuit is a function of the current discharge requirement of the VLSI circuit. Clearly, some energy is also wasted in the DC-DC converter[1]. The battery life does not have a linear relationship with the power consumption of the circuit. For example, a 2X increase in circuit power consumption may cause a 3X reduction in the battery lifetime, compared with the 2X reduction in the ideal case.

In this paper, we adopt the same energy-delay metric to evaluate low power digital designs. However, we depart from [2] by considering a first-order model of the battery sub-system which powers the VLSI circuit and show that the basic energy-delay tradeoff curve will change as a result of this integrated battery-hardware model. We thereby provide better insight into some of the basic tradeoffs that exist in battery-operated low power digital designs. We therefore show that, for battery-operated circuits, discussion of power-speed trade-off will be incomplete and inaccurate if we only consider the characteristics of the VLSI circuit.

The paper is organized as follows. Section II introduces some background knowledge. Section III gives the analytical form of the energy-delay product using an integrated battery-hardware model. Section IV presents the experimental results and discussions. Section V discusses the problem of optimal battery selection for a given VLSI circuit. Section VI gives our conclusions.

II. BACKGROUND

A. *Battery Overview*

Different types of batteries are being used in a wide range of applications [6]-[14]. They can be classified into the *primary batteries* (non-rechargeable) and the *secondary batteries* (rechargeable). Batteries can also be classified based on the electrochemical material used for their electrodes or the type of their electrolytes, e.g., Lead-acid, Ni-Cd, Ni-Zn, Ag-Zn, Zn-Air, Nickel-Metal Hydride, Lithium-Ion, Lithium-Polymer, etc.. Among these, the Nickel-Metal Hydride battery and the Lithium-Ion battery are currently the most popular batteries for portable computers.

Figure 2 taken from [6] shows the internal structure of a typical rechargeable lithium battery. It consists of the lithium foil anode, the composite cathode, and the electrolyte that serves as an ionic path between electrodes and separates the two materials. Electronic energy is generated by chemical reaction among these three components. For rechargeable batteries, applying electrical recharging can reverse chemical reaction, hence the battery can be used for multiple times (normally several hundred times).

[1] This is however relatively small and independent of the output current demand for a well-designed DC-DC converter [5].

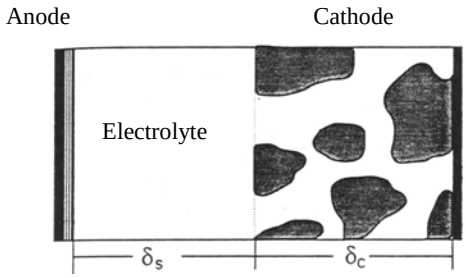

Figure 2 The internal structure of a battery

B. DC-DC Converters

Figure 3 [5] shows the block diagram of a high-efficiency DC-DC converter that can be integrated on a chip. Node BVdd is the input of the DC-DC converter which is connected to the positive electrode of the battery. Node CVdd is the output of the DC-DC converter which is connected to the VLSI circuit. The circuit level diagram for the Buck Converter is also shown. Other components are used for adaptively generating the switching signals for the Buck Converter such that the voltage at CVdd is stabilized at the target supply voltage for the VLSI circuit.

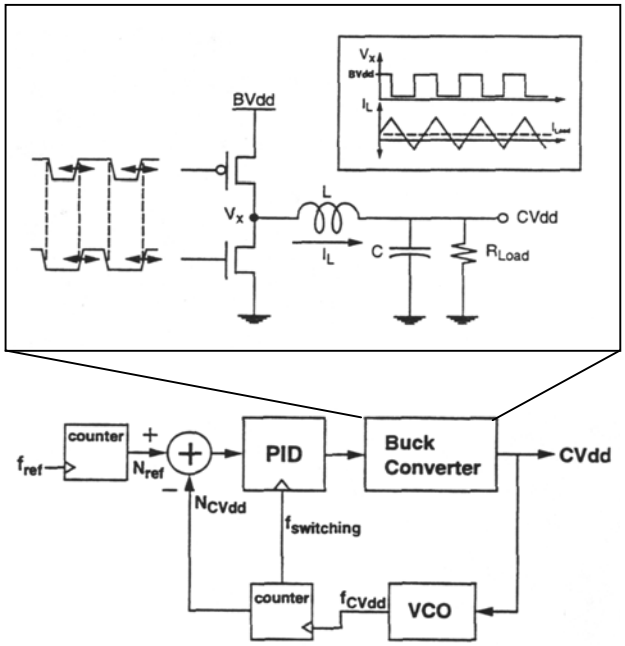

Figure 3 The structure of a DC-DC converter

C. Low Power Design Metrics

The delay of a CMOS circuit can be estimated as [1]:

$$t_d = k\frac{CV_{dd}}{(V_{dd} - V_{th})^2} \tag{2.1}$$

where k is some positive constant, C is the loading capacitance, V_{dd} is the supply voltage of the circuit, and V_{th} is the magnitude of the threshold voltage of a CMOS transistor.

The energy needed to complete an operation (e.g.. a 0→1 transition) is calculated as [1]:

$$E_{op} = nCV_{dd}^2 \tag{2.2}$$

where n is some positive constant, C is the loading capacitance, and V_{dd} is the supply voltage.

The energy-delay product (EDP) metric is then:

$$EDP_{op} = k'' \cdot \frac{V_{dd}^3}{(V_{dd} - V_{th})^2} \tag{2.3}$$

where $k'' = k \cdot n \cdot C$.

Notice that Equations (2.1), (2.2) and (2.3) are general enough such that they can used for representing t_d and E_{op} for the whole circuit and for complex operations as well as for one single gate and one single transition. Figure 4 shows energy, delay, and energy-delay product curves versus the supply voltage. The minimum value of the energy-delay product occurs at V_{dd}=3V_{th} [1].

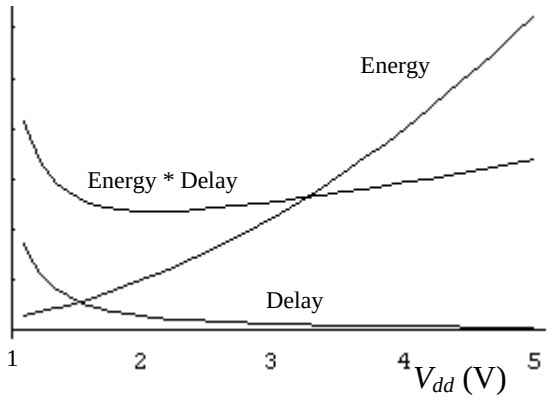

Figure 4 Energy and Delay vs. Supply Voltage (V_{th}=0.7V)

D. Battery Capacity

We define CAP_0 as the amount of energy that is stored in a new primary battery or a fully charged secondary battery. The actual capacity CAP_{act} is defined as:

$$CAP_{act} = CAP_0 \cdot \mu, \quad 0 < \mu < 1 \tag{2.4}$$

where μ is called the efficiency (or utilization) factor. CAP_{act} is the actual energy that can be output by the battery.

The efficiency factor μ is a function of discharge current I:

$$\mu = f(I) \tag{2.5}$$

where f is a monotonic-decreasing function [6]. Only the low-frequency part of the current is relevant to changing the battery efficiency [14]. Therefore, I represents the time-averaged output current of the battery. The actual capacity of the battery will decrease when the discharge current increases.

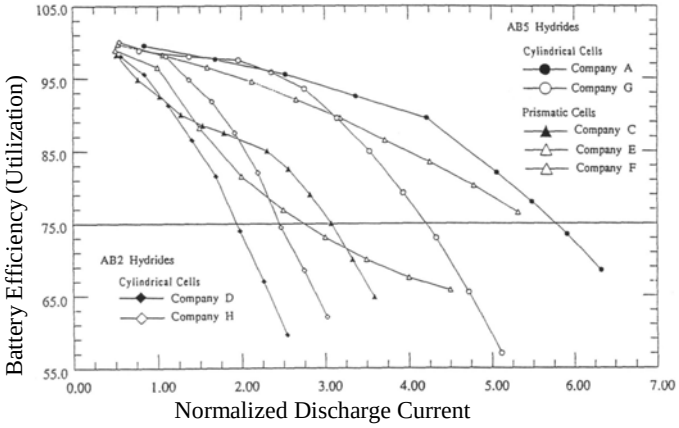

Figure 5 Efficiency factor versus discharge current

Figure 5 shows the efficiency factor versus discharge current curve for some commercial Nickel-Metal Hydride batteries [12]. Similar curves exist for lithium batteries [13].

To obtain an analytical form, two approximation functions will be used in this paper: linear and quadratic. With the linear approximation, Eqn. (2.5) is written as:

$$\mu = 1 - \alpha \cdot I \tag{2.6}$$

where α is a positive constant number.

With the quadratic approximation, Eqn. (2.5) is written as:

$$\mu = 1 - \alpha \cdot I^2 \tag{2.7}$$

III. ENERGY-DELAY PRODUCT

We first give some useful notation:

T: Clock cycle time for one operation

V_0: Output voltage of the battery

I_0: Output current of the battery

$\overline{I_0}$: Average battery current over time T

V_{dd}: Supply voltage of the circuit

I_{dd}: Supply current of the circuit

$\overline{I_{dd}}$: Average circuit current over time T

μ: Efficiency factor of the battery

η: Efficiency of the DC-DC converter

E_{op}: The ideal energy needed for one operation

E_{op}^{act} : The actual (battery) energy needed for one operation

Notice that V_0, V_{dd} and η remain constant during T.

A. The Effective Energy per Operation

From Eqn. (2.2), the energy per operation consumed by the circuit can be written as:

$$\begin{aligned} E_{op} &= nCV_{dd}^2 = \int_0^T V_{dd} \cdot I_{dd} \cdot dt \\ &= V_{dd} \cdot \int_0^T I_{dd}\, dt = V_{dd} \cdot \overline{I_{dd}} \cdot T \end{aligned} \tag{3.1}$$

Notice that actual I_{dd} is a function of time.

We can write the following equation for the DC-DC conversion:

$$\eta \cdot V_0 \cdot I_0 = V_{dd} \cdot I_{dd} \quad \text{or} \quad \eta \cdot V_0 \cdot \overline{I_0} = V_{dd} \cdot \overline{I_{dd}} \tag{3.2}$$

The actual energy per operation is calculated as:

$$E_{op}^{act} = \int_0^T \frac{V_0 \cdot I_0}{\mu} dt \tag{3.3}$$

where μ is a function of the average value of I_0. We then can write Eqn. (3.3) as:

$$E_{op}^{act} = \frac{V_0 \cdot \overline{I_0} \cdot T}{f(\overline{I_0})} \tag{3.4}$$

Substituting equations (3.1) and (3.2), we obtain:

$$E_{op}^{act} = \frac{V_0 \cdot T \cdot \dfrac{E_{op}/T}{V_0 \cdot \eta}}{f\left(\dfrac{E_{op}/T}{V_0 \cdot \eta}\right)} = \frac{1}{\eta} \cdot \frac{nCV_{dd}^2}{f\left(\dfrac{nCV_{dd}^2}{V_0 \cdot \eta \cdot T}\right)} \tag{3.5}$$

If we replace f in (3.5) by either (2.6) or (2.7), we can write the actual energy per operation as a function of the supply voltage V_{dd}. If we use Eqn. (2.6), Eqn. (3.5) becomes:

$$E_{op}^{act} = \frac{1}{\eta} \cdot \frac{nCV_{dd}^2}{1 - \alpha \cdot \dfrac{nCV_{dd}^2}{V_0 \cdot \eta \cdot T}} \tag{3.6}$$

If we use Eqn. (2.7), we get:

$$E_{op}^{act} = \frac{1}{\eta} \cdot \frac{nCV_{dd}^2}{1 - \alpha \cdot \left(\dfrac{nCV_{dd}^2}{V_0 \cdot \eta \cdot T}\right)^2} \tag{3.7}$$

From (3.6) and (3.7), we know that the actual energy dissipation E_{op}^{act} is always larger than the ideal energy dissipation E_{op}. The larger the V_{dd} is, the larger is the difference. Figure 6 shows the comparison of E_{op} and E_{op}^{act} as a function of V_{dd}.

Due to space limitation, we use Eqn. (3.6) for the rest of the analysis in the section. Analysis using Eqn. (3.7) is similar.

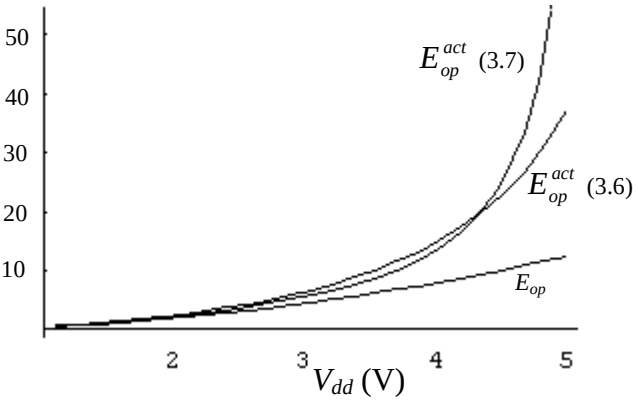

Figure 6 Comparison of E_{op} and E_{op}^{act}

B. The Energy-Delay-Product Metric

The energy-delay product (in brief, EDP) can be written as:

$$EDP_{op}^{act} = k \cdot \frac{V_{dd}}{(V_{dd} - V_{th})^2} \cdot \frac{1}{\eta} \cdot \frac{nCV_{dd}^2}{1 - \alpha \cdot \dfrac{nCV_{dd}^2}{V_0 \cdot \eta \cdot T}} \tag{3.8}$$

or

$$EDP_{op}^{act} = k' \cdot \frac{V_{dd}^3}{(V_{dd} - V_{th})^2 (1 - \beta V_{dd}^2)} \tag{3.9}$$

where

$$k' = \frac{k \cdot n \cdot C}{\eta} \quad \text{and} \quad \beta = \frac{\alpha \cdot n \cdot C}{V_0 \cdot \eta \cdot T}$$

To give a quantitative comparison between EDP_{op} and EDP_{op}^{act}, we assign reasonable values to the parameters as follows: η, the efficiency of the DC-DC converter, is taken to be 90% [5], V_{th}=0.7V and V_0=4V. Assuming a circuit with V_{dd}=3.3V and average power dissipation of 33W, we obtain (nC/T)=3. α=0.05 is a reasonable value for the battery (50% efficiency at a 10A discharge current) [12]. Therefore, a reasonable value for β is around 0.04[2]. Since the absolute value of k' and k" does not influence the solution of V_{dd} for minimum EDP, we set k"=1, therefore k'=1/0.9. Figure 7 shows the plots of EDP_{op} and EDP_{op}^{eff} for different β values. Table 1 shows the solution for V_{dd} values that minimize the EDP.

The analytical derivation indicates that after combining the battery system with the VLSI circuit, the optimal V_{dd} for minimum energy-delay product becomes smaller than the ideal case that does not consider the battery system. The optimal V_{dd} may change depending on the discharge characteristics of the battery. A larger β implies a larger value of α, which means the battery efficiency decreases faster when the current increases. Therefore, we conclude that when α increases, the value of optimal V_{dd} becomes smaller. For the typical β value of 0.04, the optimal V_{dd} is 17% smaller than the optimal V_{dd} for the ideal case.

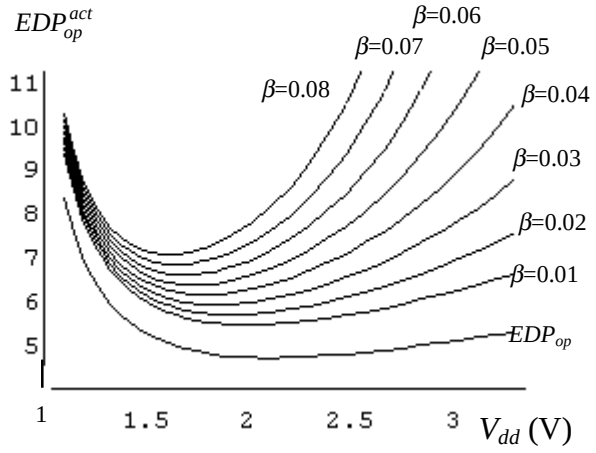

Figure 7 Plots of EDP_{op} and EDP_{op}^{act} with different β values

Table 1 Solution of V_{dd} for minimum EDP

	EDP_{op}	EDP_{op}^{act}							
β		0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08
V_{dd}*(V)	2.1	2.0	1.9	1.8	1.75	1.71	1.68	1.66	1.65

IV. EXPERIMENTAL RESULTS

For the experimental setup, we designed a small system where the VLSI circuit is represented by an optimally sized 4-inverter buffer with a capacitive load of 0.5pF. A 0.5µ CMOS process technology was used for the transistor models. A macro-model of the battery was generated following the model proposed by [14]. The battery capacity was scaled down to reduce the simulation time, as well as to match the scaled-down size of the VLSI circuit. An appropriate macro-model was used for the DC-DC converter simulation. The efficiency of the converter was set to 90% for converting V_0 to different V_{dd}'s. We used HSPICE to generate the experimental results.

[2] The value for β must satisfy: $0 < 1 - \beta V_{dd}^2 < 1$.

A. *Ideal Battery Model*

To obtain the various curves for the ideal case, we simulated the circuit for one clock cycle with an ideal voltage source with different V_{dd} values. Energy and delay values were measured during the simulation, energy-delay product values were subsequently calculated from these. The plots of these metrics versus V_{dd} are shown in Figure 8.

Experimental results show that the V_{dd} for minimum energy-delay product is about 2.0V, which is close to the analytical result (2.1V).

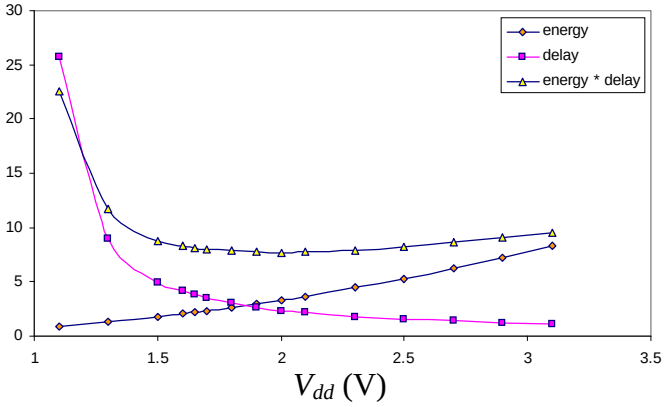

Figure 8 Energy (pJ), delay (ns), energy-delay (pJ*ns) plots for the ideal battery model

B. *Real Battery Model*

In this setup, we want to measure the actual energy per operation E_{op}^{act} for the system. Then we can use the delay measurement from the previous sub-section to obtain the plot of the actual energy-delay product EDP_{op}^{act}. Since we could not measure an abstract quantity directly, we use the following relation:

$$E_{op}^{act} = \frac{CAP_0}{N} \qquad (4.1)$$

where N represents the number of operations that the circuit performs before the battery is depleted. It can easily be measured by simulation. Batteries with different α values are simulated to make similar plots as in Figure 7 and Table 1. The results are reported in Figure 9 and Table 2.

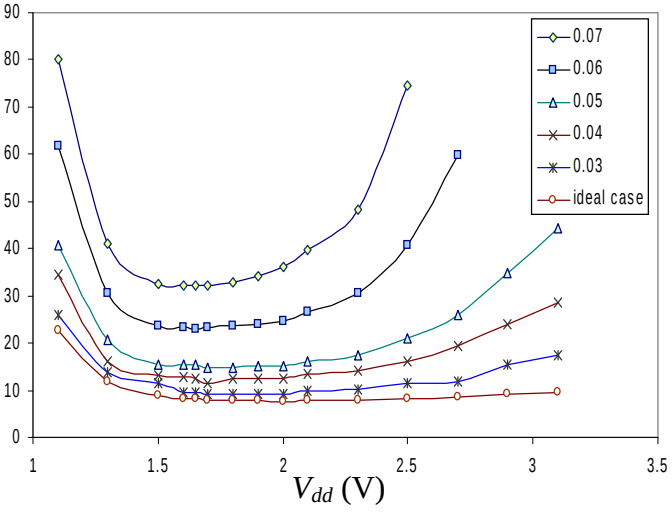

Figure 9 Plots of EDP_{op} and EDP_{op}^{act} (pJ*ns)

Table 2 Optimal V_{dd} from experimental results

	EDP_{op}	EDP_{op}^{act}				
β		0.03	0.04	0.05	0.06	0.07
V_{dd}*(V)	2.0	1.9	1.75	1.7	1.65	1.6

V. BATTERY SELECTION

We showed in the previous section that the battery characteristics change the optimal value of V_{dd} for a VLSI circuit. Similarly, the characteristics of the VLSI circuit can influence choice of the battery for the circuit. The goal of battery selection process is to find the battery that can make the given system work longest within one battery cycle (time from new or fully charged battery to battery replacement or recharge). If we define the battery life as the number of operations the system can perform before the battery is totally discharged, our goal is to find the battery which maximizes N as defined in Section IV. Of course there are other considerations for battery selection such as weight and size. We assume that those constraints have also been considered for the selection of the appropriate battery and that we have a tie with respect to those criteria.

Under the ideal battery model, we have:

$$N = \frac{CAP_0}{E_{op}} \tag{5.1}$$

Since E_{op} is known (and fixed) for the given circuit, to maximize N, we must simply maximize CAP_0. Therefore, the criterion for battery selection is very simple: select the battery with maximum capacity CAP_0.

Under the real battery model, we have:

$$N = \frac{CAP_0}{E_{op}^{act}} \tag{5.2}$$

Substituting Eqn. (3.6) into (5.2) and noting that η, V_{dd}, I_{dd} , and T have been determined by the design of the DC-DC converter and the VLSI circuit, we can rewrite (5.2) as:

$$N = \frac{CAP_0 \cdot (1 - \frac{\alpha}{V_0} \cdot k)}{k \cdot T} \tag{5.3}$$

where $k = \frac{V_{dd} \cdot \overline{I_{dd}}}{\eta}$ is the amount of battery output power required by the DC-DC converter.

From Eqn. (5.4), we can see that to maximize N, we need to maximize $CAP_0 \cdot (1 - \frac{\alpha}{V_0} \cdot k)$. Recall that α and V_0 are important performance parameters for batteries. Therefore, a battery with the largest CAP_0 may not be the best choice. As an example, if all candidate batteries have the same CAP_0, we should choose the one with smallest value of α/V_0.

VI. CONCLUSION

In this paper, we showed that it is essential to consider the characteristics of the battery that powers a portable electronic circuit in deciding the effectiveness of various low power optimization techniques. We also proposed a simple, yet accurate, integrated model of the battery and VLSI sub-systems. Next we studied (analytically and empirically) the problem of assigning a voltage level to the VLSI circuit which minimizes the effective (actual) energy-delay product in the combined system. Finally we considered the problem of battery selection for given VLSI circuit (with fixed supply voltage level and energy per operation cost). Next step is to consider the battery-hardware co-design problem for battery-powered electronic systems.

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