An Integrated Cell Placement and Interconnect Synthesis Tool for Large-scale SFQ Logic Circuits

3EPo1C-03 [116]

S. Nazar Shahsavani[1], A. Shafaei[1], C. J. Fourie[2], M. Pedram[1]

[1]Department of Electrical Engineering, University of Southern California, Los Angeles, CA

[2] Department of Electrical and Electronic Engineering, Stellenbosch University, Stellenbosch, South Africa

1. Focus of this Poster

- Development of an integrated placement and routing methodology for RSFQ circuits considering layout issues (signal and clock routing)

2. Introduction

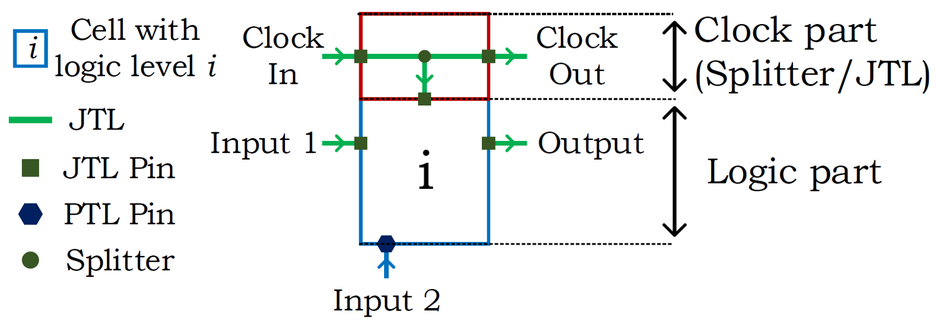
- We present a new design methodology (including cell placement, clock tree synthesis, and signal routing) based on fixed-height, but variable-width logic cell layouts.
- With our method, clock lines are routed in dedicated channels above cell rows to allow localized clock-follow-data or counter-flow-clocking implementations.
- The objective of our placement tool is to reduce the total wire length and more importantly minimize the cost of clock routing in large-scale SFQ circuits.

3. Standard Cells

• An SFQ standard cell in our library is composed of two parts:

I. A **logic design** part, which implements a Boolean function such as AND, OR, INV, etc.

II. A **built-in clock distribution** part, which is placed above the logic part and contains a splitter to provide the clock signal to the corresponding logic part, and also to pass the clock pulse to the successor cell in the logic level order. If the logic part does not need a clock signal (e.g., splitter or merger), the clock part implements a JTL to pass the clock pulse to the next cell.



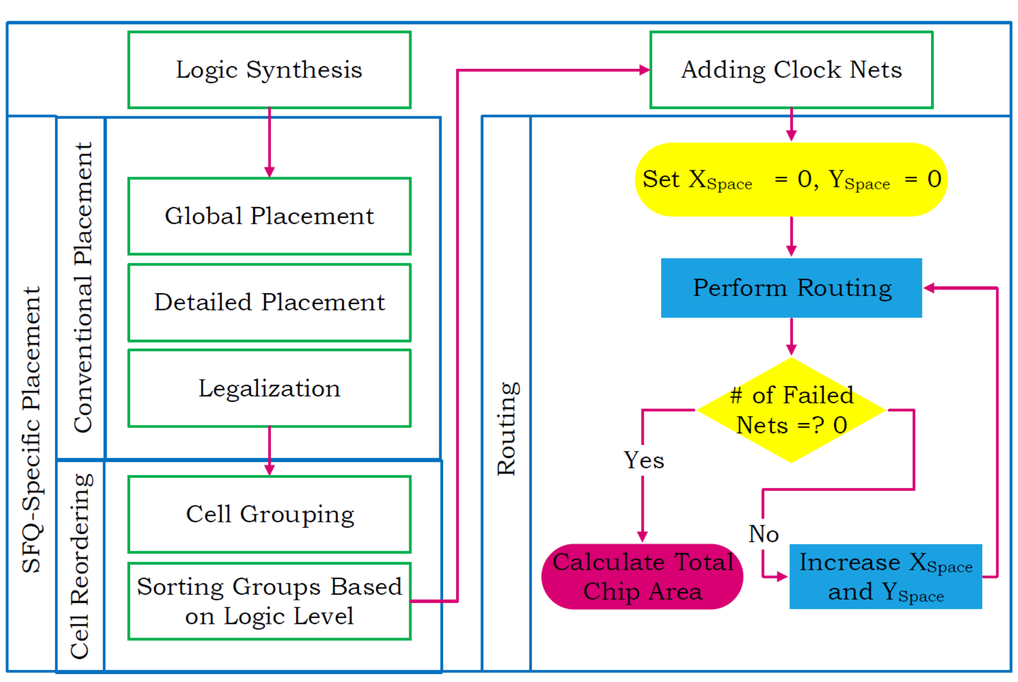
• There are two types of clock cell templates:

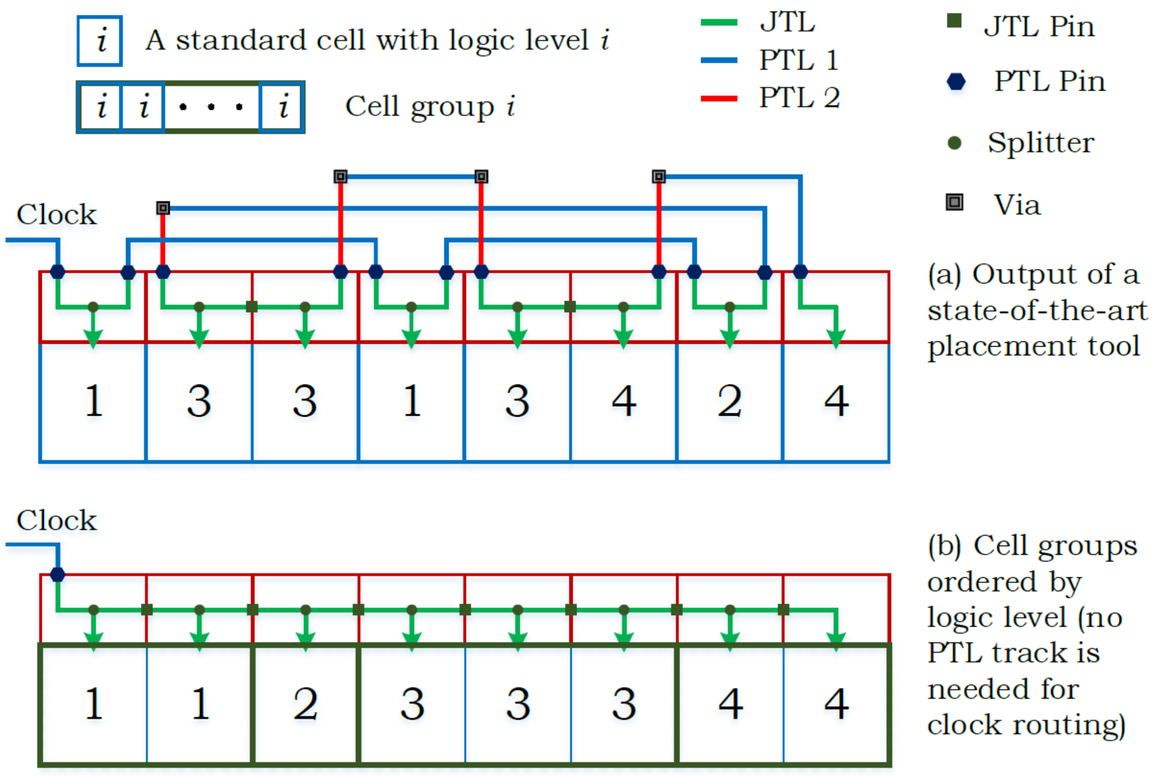
I. Pass-through cells distribute the clock signal to the next cell in the ascending order of the logic level. These templates contain either a splitter (if the corresponding logic part needs a clock signal) or a JTL (if the corresponding logic part is a splitter or a merger), and their difference is in the type (JTL or PTL) of the input/output pins.

II. End-of-line cells terminate the clock signal and differ in the type of the input pin.

4. Our Approach

- Initially, logic synthesis is performed to obtain logic levels of cells.
- Row-based placement methodology produces a legalized solution.
  - All rows will have the same height (since the height of standard cells is fixed).
  - Cells in the netlist (including splitters) are placed in a row.
  - A placement solution with the minimum wirelength is obtained using a force-directed global optimization based on **SimPL** placement algorithm.
  - Force-directed placements reduce the placement problem to that of solving a set of simultaneous linear equations to determine equilibrium (i.e., zero-force) locations for cells based on Hooke's law analogy.
  - Linear equations are solved using Conjugate Gradient method.
- SFQ-specific placement: Cells are grouped based on their logic level and cell groups in each row are sorted in the non-decreasing order of their levels.
  - No PTL for clock routing is needed since cells in each row are now placed based on the same order that they should receive the clock, and hence clock is propagated by splitters.
- Clock channels are added above each row for clock signal routing with JTLs/splitters. Symmetric design of variable-length JTLs/Splitters allows both concurrent and counter flow clocking.
- Signal routing among cells is done either by direct connection between adjacent cells and/or routing with PTLs. Cell layout supports direct tiling and/or direct access to PTL routing channels.
- Signal routing connects data signals.
  - Initially, the (horizontal) space between adjacent cells (X_{Space}) and the (vertical) space between rows (Y_{Space}) are set to zero.
  - Number of failed nets is reported. If there are no failed nets, the minimum chip area is obtained.
  - If router has failed connecting some nets, X_{Space} and Y_{Space} are increased and routing is performed again until there is no failed net. A binary search method is performed to obtain the minimum chip area.



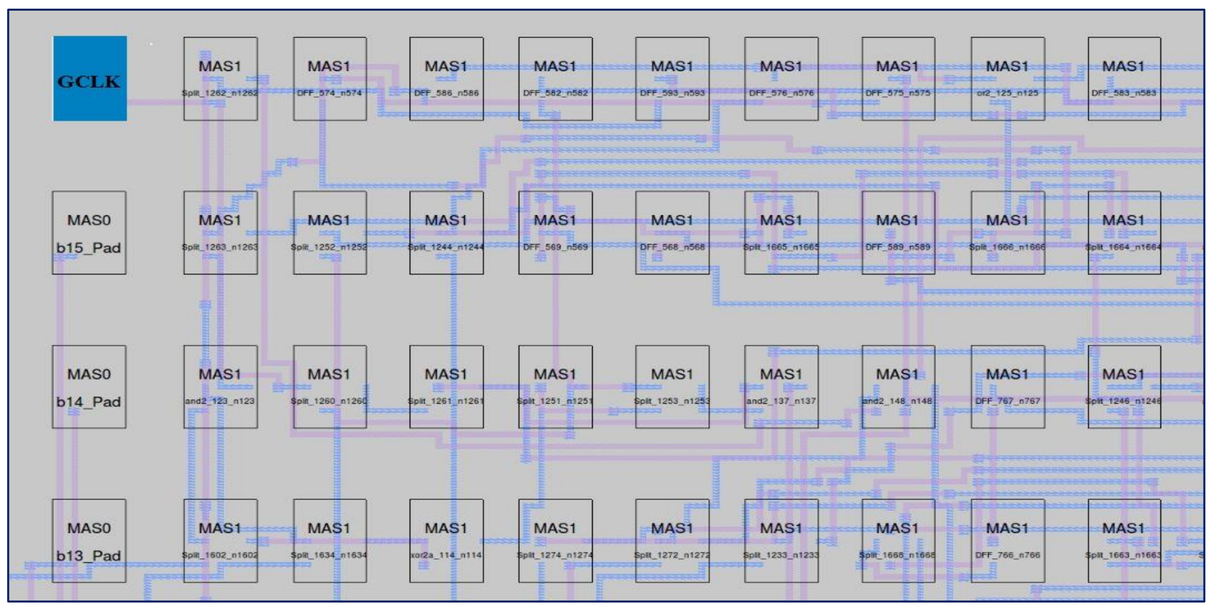


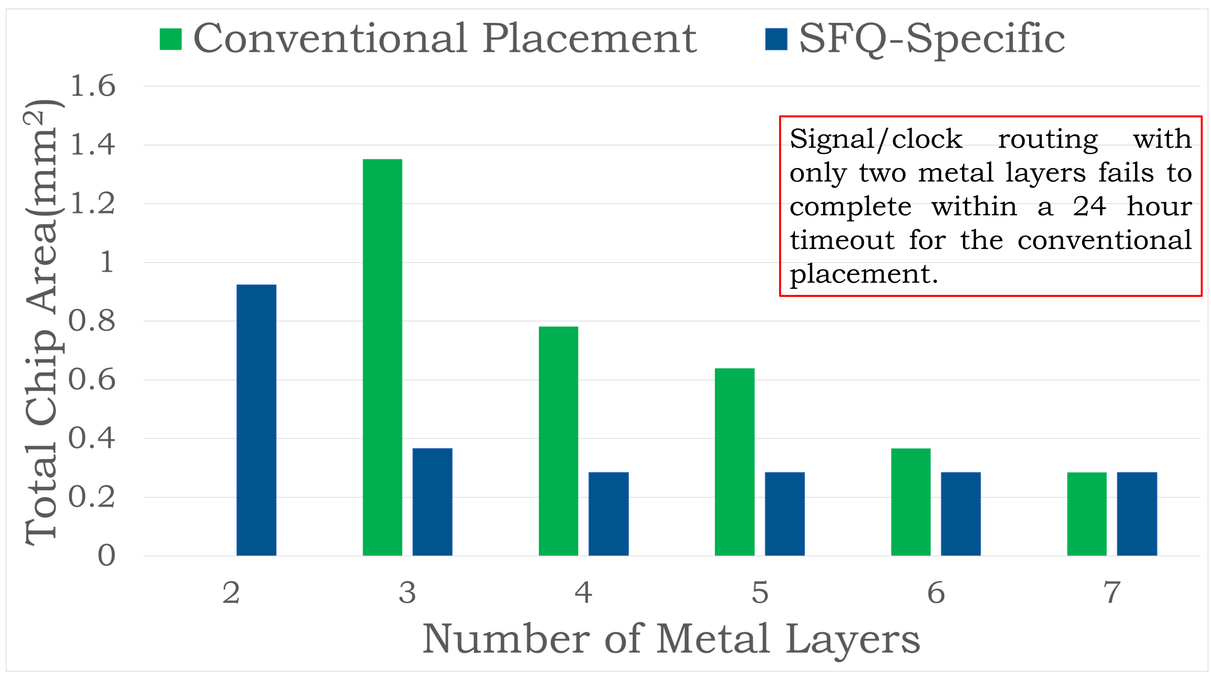
5. Benefits of this Approach

- Distribution of the clock signal to each logic cell is simplified.
- Placement can be done without having to plan for routing with JTL.
- Bias line tapped at defined locations; it does not interfere with routing.
- Process can be automated and extended to eSFQ and ERSFQ.

6. Experimental Results

- We have tested our placement and routing algorithms on a 32-bit Kogge-Stone adder, and generated final routing results for two different placements: (i) **conventional** placement, and (ii) **SFQ-specific** placement.
- The total number of cells and data nets in the aforesaid adder are 1669 and 2072, respectively.
- The total number of PTL wires added for clock routing are as follows:
  - Only one PTL for SFQ-specific placement. More specifically, this PTL wire (called the global clock, and denoted by GCLK) is used to distribute the clock signal to all cells with the minimum level in each row. The rest of clock signals are connected by splitters/JTLs to corresponding cells.
  - 1114 nets for the conventional placement.
- SFQ-specific placement tool results in 36% larger half-perimeter wirelength compared with the conventional placement.
- Because of using only one PTL track for clock routing in the SFQ-specific placement, the minimum chip area is achieved with **four** metal layers using the SFQ-specific placement, whereas the conventional placer needs **seven** metal layers to achieve the same chip area.





7. Acknowledgements

• This research project is supported by IARPA contract FA8750-15-C-0203-IARPA-BAA-14-03.

nazarsha@usc.edu, shafaeib@usc.edu, coenrad@sun.ac.za, pedram@usc.edu